Getting started with STM32 MCU hardware development.

INTRODUCTION

STM32 Hardware
. Power supply, clock, Boot , debugging
.
.
, STM32 L0, L1, F0, F1, F2, F3, F4
, Application note / Data sheet / User Manual .

Contents

Figures

Tables

1 Power supplies

1.1 Introduction

STM32 MCU / .

- VDD(*1.65V ~ 3.6 V) : Digital I/O regulator . Package VDD .

  * Data sheet .

  * VDD 1.8V Brownout reset/Power Down reset .

- VDDA(*1.7V ~ 3.6 V) : ADC, DAC, Comparators , Reset, RC oscillators, PLL .

  * VDDA , condition Data sheet .

- Vref+(*1.7V ~ VDDA) : ADC, DAC data conversion . AD, DA application VDDA . Vref+ package pin .

  * Vref+ , condition Data sheet .

- Vbat(*1.65V ~ 3.6 V) : RTC, Backup register, Backup SRAM . Application battery , VDD .

  * Vbat , condition Data sheet .

- VCAP : core, memory digital peripherals voltage regulator output load capacitor pin . , device regulator , core (BYPASS_REG).

- pin : device data sheet “Getting started with STM32xxx hardware development” pin .
    - VDD_USB
    - VLCD, VLCDrail1, VLCDrail2, VLCDrail3
    - VDDIO2
    - VREFSD+, VREFSD-, VDDSD, VDDSD12, VDDSD3, VSSSD

1.2 Power supply schemes

MCU VDD .

Figure 1 .

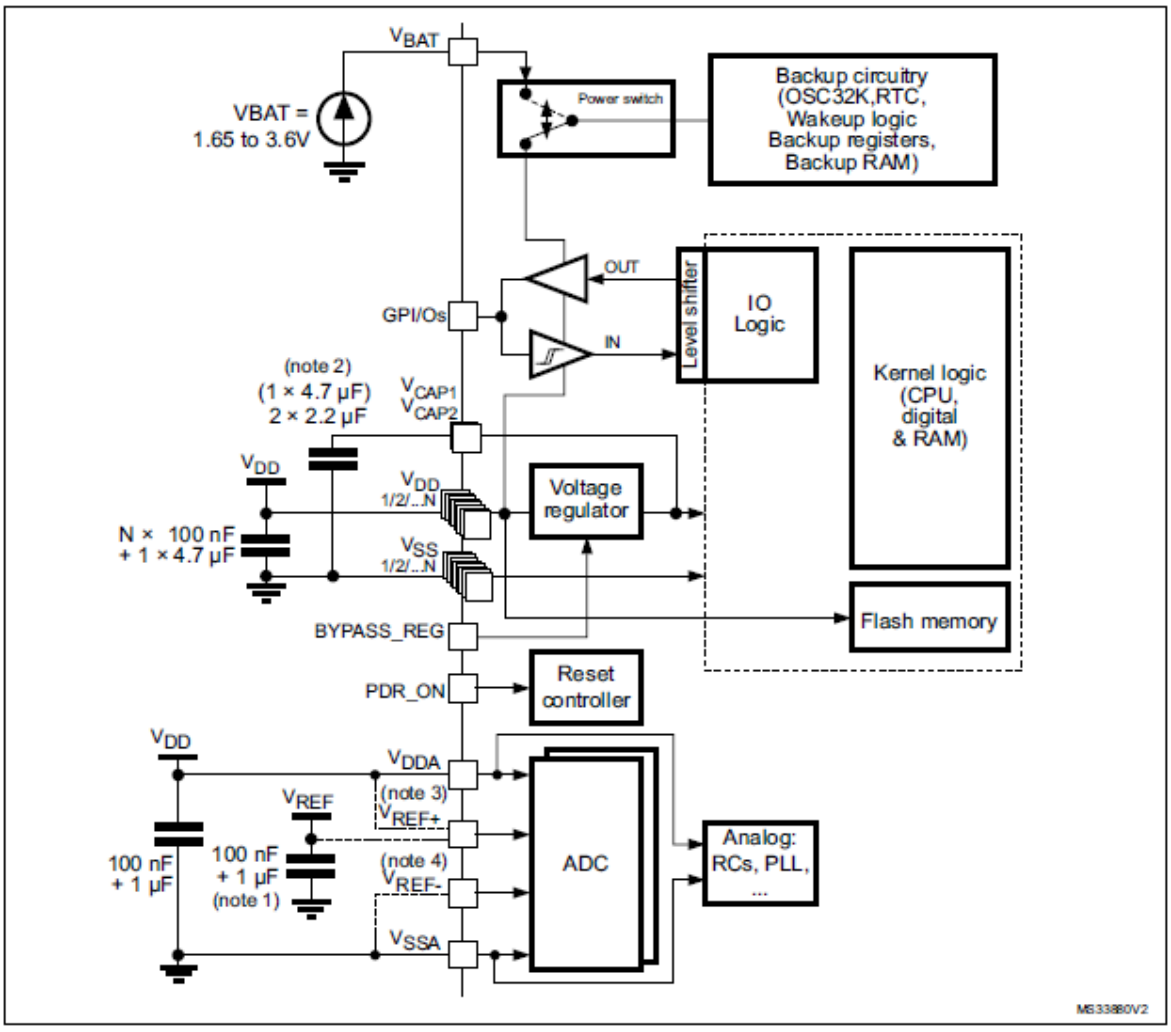


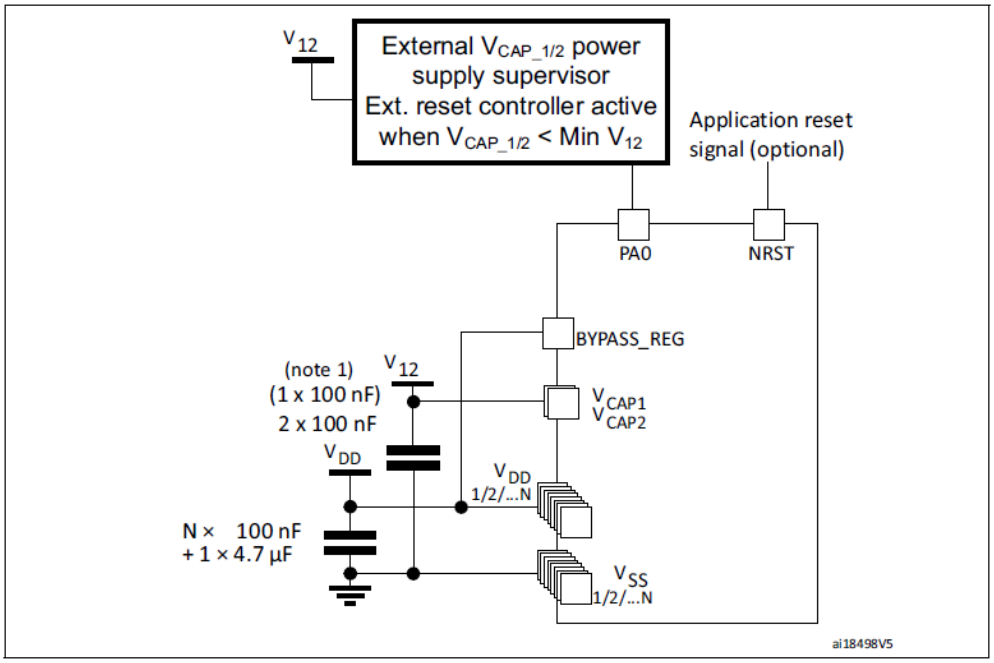
Figure 1. Power supply scheme : example of STM32F4xx

- VDD pin device 4.7uF~10uF Tantal Ceramic capacitor VDD pin 100nF capacitor .
- VDDA pin 1uF Tantal Ceramic capacitor 100nF capacitor .

- Vref+ pin 1uF~10uF Tantal Ceramic capacitor 100nF capacitor .

- VBAT pin . , VBAT pin VDD , 100nF capacitor .

- VCAP : VCAP pin 4.7uF, VCAP pin 2.2uF Ceramic capacitor .
  *( ) Regulator OFF mode Figure 2 Vcore (1.2V) VCAP pin , pin 100nF capacitor . control
  .



1. V_{CAP2} is not available on all packages. In that case, a single 100 nF decoupling capacitor is connected to V_{CAP1}

Figure 2. BYPASS_REG supervisor reset connection

1.3 Device Power supply range

Table 1, 2, 3 STM32 VDD, VDDA, Vref, Vbat range .

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Device		L0	L1	F0
VDD condition	Full speed	1.71V ≤ VDD ≤ 3.6V	2.0V ≤ VDD ≤ 3.6V	2.0V ≤ VDD ≤ 3.6V
	Range 2	1.65V ≤ VDD ≤ 3.6V	1.65V ≤ VDD ≤ 3.6V	
	Range 3	1.65V ≤ VDD ≤ 3.6V	1.65V ≤ VDD ≤ 3.6V	
VDDA condition	ADC USED	1.8V ≤ VDDA = VDD ≤ 3.6V	1.8V ≤ VDDA = VDD ≤ 3.6V	2.4V & VDD ≤ VDDA ≤ 3.6V *(VDD-VDDA < 0.4V)
	ADC not USED	1.65V ≤ VDDA = VDD ≤ 3.6V	1.65V ≤ VDDA = VDD ≤ 3.6V	2.0V & VDD ≤ VDDA ≤ 3.6V
Vref+ condition	ADC USED	1.8V ≤ Vref+ ≤ VDDA	2.4 V ≤ VREF+ = VDDA (full speed) 1.8 V ≤ VREF+ = VDDA (500Ksps) 2.4 V ≤ VREF+ < VDDA (500Ksps) 1.8 V ≤ VREF+ < VDDA (250Ksps)	N.A
	ADC not USED	0V ≤ Vref+ ≤ VDDA	0V ≤ Vref+ ≤ VDDA	
Vbat condition		1.65V ≤ Vbat ≤ 3.6V	1.65V ≤ Vbat ≤ 3.6V	1.65V ≤ Vbat ≤ 3.6V

Table 1. Power supply range : L0, L1, F0

Device		F1	F2	F3
VDD condition	Full speed	2.0V ≤ VDD ≤ 3.6V	1.8V ≤ VDD ≤ 3.6V 1.65V ≤ VDD ≤ 3.6V (WLCSP only)	2.0V ≤ VDD ≤ 3.6V
	Range 2			
	Range 3			
VDDA condition	ADC USED	2.4V ≤ VDDA = VDD ≤ 3.6V	2.0V ≤ VDDA = VDD ≤ 3.6V (2Msps) 1.8V ≤ VDDA = VDD ≤ 3.6V (1Msps)	2.4V ≤ VDDA ≤ 3.6V *(VDD-VDDA < 0.4V)
	ADC not USED	2.0V ≤ VDDA = VDD ≤ 3.6V	1.8V ≤ VDDA = VDD ≤ 3.6V	2.0V ≤ VDDA ≤ 3.6V
Vref+ condition	ADC USED	2.4 V ≤ VREF+ ≤ VDDA	1.8V ≤ Vref+ ≤ VDDA	2.0V ≤ Vref+ ≤ VDDA (F30x) 2.4V ≤ Vref+ ≤ VDDA (F37x, F38x)
	ADC not USED		1.65V ≤ Vref+ ≤ VDDA	Vref+ = VDDA 0V ≤ Vref+ ≤ VDDA (F383)
Vbat condition		1.8V ≤ Vbat ≤ 3.6V	1.8V ≤ Vbat ≤ 3.6V	1.65V ≤ Vbat ≤ 3.6V

Table 2. Power supply range : F1, F2, F3

Device		F4	F7
VDD condition	Full speed	1.8V ≤ VDD ≤ 3.6V 1.7V ≤ VDD ≤ 3.6V (in restrict condition)	TBD
	Range 2		
	Range 3		
VDDA condition	ADC USED	2.4V ≤ VDDA = VDD ≤ 3.6V (2.4Msps) 1.8V ≤ VDDA = VDD ≤ 2.4V (1.2Msps) 1.7V ≤ VDDA = VDD ≤ 3.6V (in restrict condition)	TBD
	ADC not USED	N.D	TBD
Vref+ condition	ADC USED	1.7 V & (VDDA-1.2V) ≤ VREF+ ≤ VDDA	TBD
	ADC not USED	1.65V ≤ Vref+ ≤ VDDA	TBD
Vbat condition		1.65V ≤ Vbat ≤ 3.6V	1.65V ≤ Vbat ≤ 3.6V

Table 3. Power supply range : F4, F7

1.4 Power supply supervisor

STM32 **POR/PDR**(Power On Reset/Power Down Reset), **BOR**(Brown Out Reset), **PVD**(Programmable Voltage Detector)

. Table 4. Power supply supervisor

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*( ) PDR BOR device data sheet “Getting started with STM32xxx hardware development”

.

Device		L0	L1	F0	F1
POR/PDR	threshold (Max)	1.65V	1.65V	2.0V	2.0V
	hysteresis	? mV	? mV	40 mV	40 mV
	generate	reset	reset	reset	reset
	Active	Always	Always	Always	Always
BOR	Range	1.8V ~ 3.0V	1.8V ~ 3.0V	-	-
	Number of thresholds	5	5	-	-
	hysteresis	40mV or 100mV	40mV or 100mV	-	-
	generate	reset	reset	-	-
	control	option bytes	option bytes	-	-
	Active	option bytes	option bytes	-	-
PVD	Range	1.85V ~ 3.05V	1.85V ~ 3.05V	2.08V ~ 2.78V	2.08V ~ 2.78V
	Number of thresholds	7	7	8	8
	hysteresis	100mV	100mV	100mV	100mV
	generate	interrupt	interrupt	interrupt	interrupt
	control	software	software	software	software
Device		F2	F3	F4	F7
POR/PDR	threshold (Max)	1.8V	2.0V	1.8V	TBD
	hysteresis	40 mV	40 mV	40 mV	TBD
	generate	reset	reset	reset	TBD
	Active	Always	Always	by PDR_ON pin	TBD
BOR	Range	1.8V ~ 2.97V	-	1.8V ~ 2.97V	TBD
	Number of thresholds	3	-	3	TBD
	hysteresis	100mV	-	100mV	TBD
	generate	reset	-	reset	TBD
	control	option bytes	-	option bytes	TBD
	Active	option bytes	-	option bytes	TBD
PVD	Range	2.04V ~ 3.03V	2.08V ~ 2.78V	2.04V ~ 3.03V	TBD
	Number of thresholds	8	8	8	TBD
	hysteresis	100mV	100mV	100mV	TBD
	generate	interrupt	interrupt	interrupt	TBD
	control	software	software	software	TBD

Table 4. Power supply supervisor

1.5 System reset

STM32 reset . EMS

Figure 3 100nF pull-down capacitor reset

.

*( ) NRST pin **Open-drain** output port

. push-pull output port

(WWDG, IWDG, Power Reset, Software Reset…)

(HW/SW) .

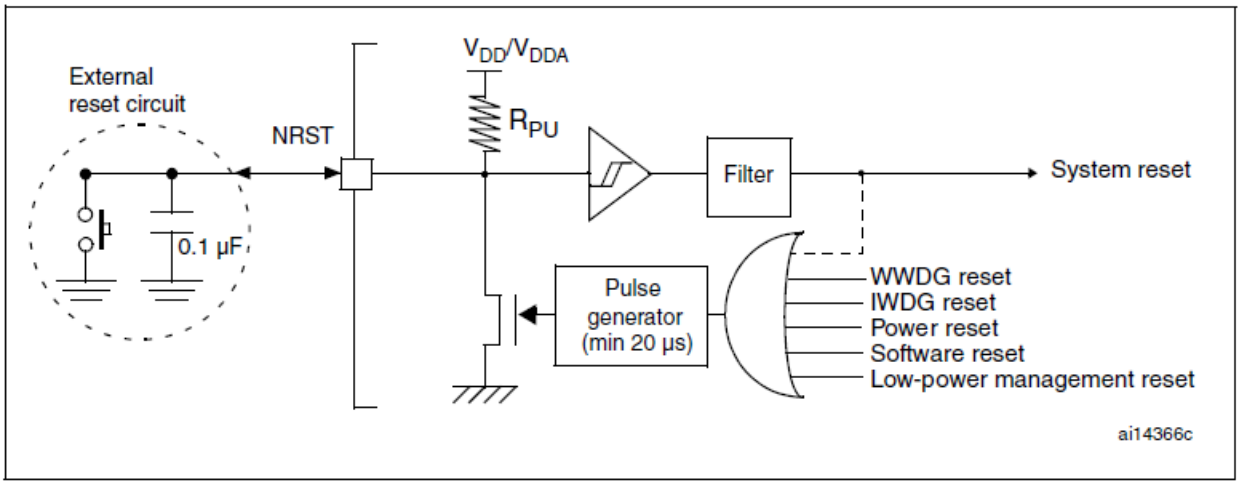

Figure 3. Reset circuit

2 Clocks

2.1 Introduction

STM32 clock system clock(SYSCLK) .

- HSI (High Speed Internal clock)
- HSE (High Speed External clock)
- PLL
- MSI (Multi Speed Internal clock) (device)

STM32 clock secondary clock .

- LSI (Low Speed Internal clock) : Device 32KHz, 37KHz, 40KHz LSI IWDG, RTC .
- LSE (Low Speed External clock) : External clock crystal clock , RTC clock .
- HSI 14MHz (14MHz High Speed Internal clock) (device) : ADC clock .
- HSI48 (48MHz High Speed Internal clock) (device) : USB Random number generator .

  HSI48 clock device crystal oscillator USB .

2.2 HSE

HSE clock source clock .

- HSE user external clock (Figure 4)
- HSE external crystal/ceramic resonator (Figure 5)

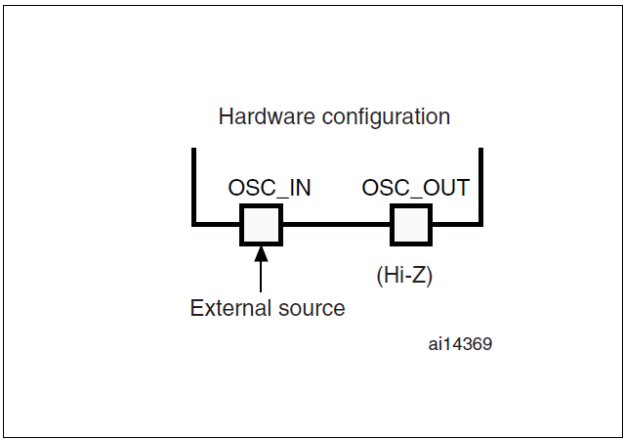

Figure 4. External clock

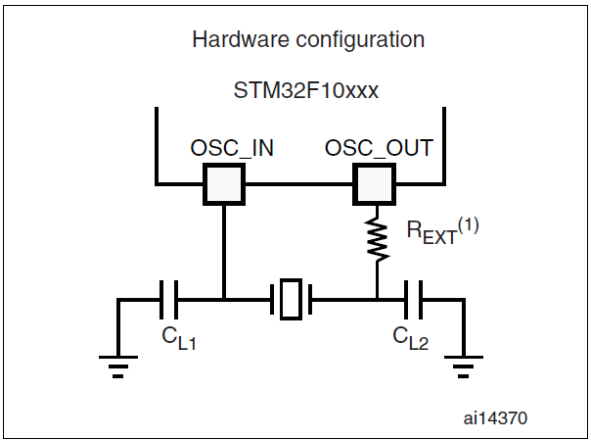

Figure 5. Crystal/ceramic resonators

2.2.1 External source (HSE bypass)

Device HSE clock speed . HSE clock

device data sheet .

*( ) External clock source 50% duty , OSC_IN pin

. OSC_OUT pin hi-impedance (N.C) .

2.2.2 External crystal/ceramic resonator (HSE crystal)

Device crystal frequency . HSE crystal/ceramic resonator

device data sheet .

*( ) crystal CL1, CL2 crystal impedance

. Crystal “AN2867 : Oscillator design guide for ST microcontrollers” .

2.3 LSE

LSE clock source clock .

- LSE user external clock (Figure 6)
- LSE external crystal/ceramic resonator (Figure 7)

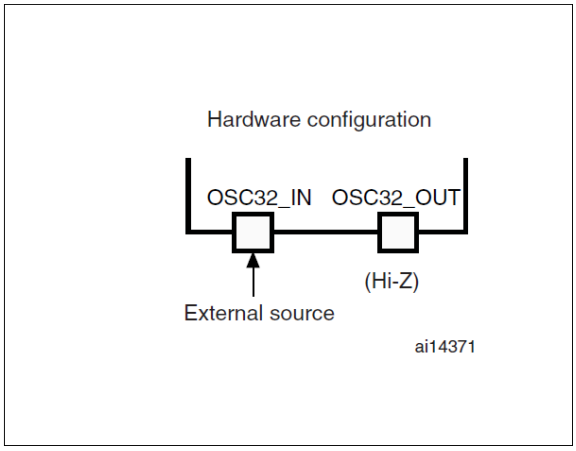

Figure 6. External clock

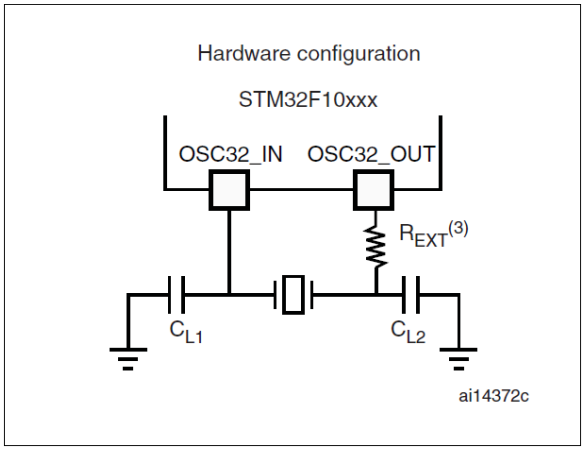

Figure 7. Crystal/ceramic resonators

2.3.1 External source (LSE bypass)

Device LSE clock speed . LSE clock

device data sheet .

*( ) External clock source 50% duty , OSC32_IN pin

. OSC32_OUT pin hi-impedance (N.C) .

2.3.2 External crystal/ceramic resonator (LSE crystal)

Device crystal frequency . LSE crystal/ceramic resonator

device data sheet .

*( ) crystal CL1, CL2 crystal impedance

. Crystal “AN2867 : Oscillator design guide for ST microcontrollers” .

3 Boot

3.1 Introduction

STM32 Table 5 3 boot mode . Boot mode
Main flash memory application binary download /
. , application FW update STM32
System boot loader . User IAP
.

Boot mode selection		Boot mode	Aliasing
BOOT1(1)	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

Table 5. Boot modes

- Main Flash memory : application binary memory
  application code boot mode Main flash memory
  .
- System memory : STM32 memory System boot loader
  boot mode System memory .
- Embedded SRAM : Reset STM32 SRAM code
  boot mode Embedded SRAM .

3.2 Boot mode

STM32 Boot mode BOOT0, BOOT1 HW
. BOOT0, BOOT1 pin Table 5 BOOT0, BOOT1 .
Figure 8 boot mode .

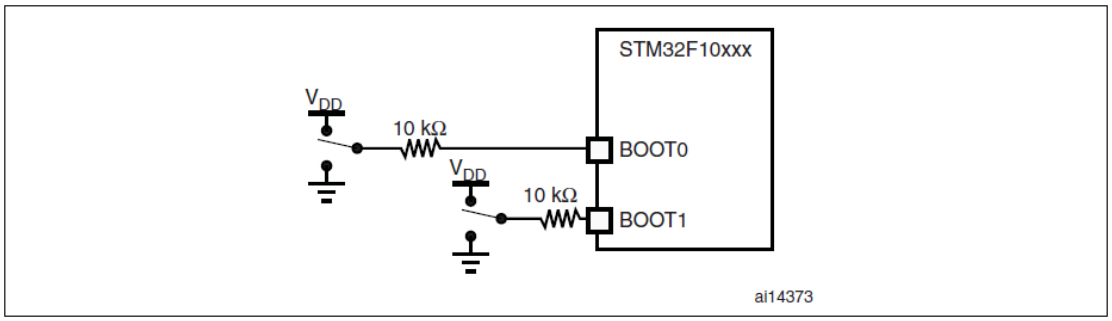

Figure 8. Boot mode selection implementation example

(F0, F3, L0 series) BOOT1 HW .

BOOT1 Option byte nBOOT1 bit . nBOOT1 bit BOOT1 latch . , nBOOT1 bit '1' BOOT1 '0' Main flash memory System memory booting .

* BOOT0, BOOT1 reset Standby mode 4 SYSCLK rising edge latch .

3.3 System boot loader

System bootloader STM32 device System memory . USART, CAN, USB, I2C, SPI, … protocol , protocol pin datasheet "AN2606 : STM32 microcontroller system memory boot mode" .

Figure 9, 10 boot loader . System bootloader .

STM32 series	Device		Supported serial peripherals	Bootloader ID		Bootloader (protocol) version
				ID	Memory location	
F0	STM32F051xx		USART1/USART2	0x21	0x1FFFF7A6	USART (V3.1)
	STM32F031xx		USART1	0x10	0x1FFFF7A6	USART (V3.1)
	STM32F042xx		USART1/USART2/ I2C1/ DFU (USB Device FS)	0xA0	0x1FFFF6A6	USART (V3.1) DFU (V2.2) I2C (V1.0)
	STM32F072xx		USART1/USART2/ I2C1/ DFU (USB Device FS)	0xA1	0x1FFFF6A6	USART (V3.1) DFU (V2.2) I2C (V1.0)
F1	STM32F10xxx	Low-density	USART1	NA	NA	USART (V2.2)
		Medium-density	USART1	NA	NA	USART (V2.2)
		High-density	USART1	NA	NA	USART (V2.2)
		Medium-density value line	USART1	0x10	0x1FFFF7D6	USART (V2.2)
		High-density value line	USART1	0x10	0x1FFFF7D6	USART (V2.2)
	STM32F105xx/107xx		USART1 / USART2 (remapped) / CAN2 (remapped) / DFU (USB Device)	NA	NA	USART (V2.2(1)) CAN (V2.0) DFU(V2.2)
	STM32F10xxx XL-density		USART1/USART2 (remapped)	0x21	0x1FFFF7D6	USART (V3.0)
F2	STM32F2xxxx		USART1/USART3	0x20	0x1FFF77DE	USART (V3.0)
			USART1/USART3/ CAN2/ DFU (USB Device FS)	0x33	0x1FFF77DE	USART (V3.1) CAN (V2.0) DFU (V2.2)
F3	STM32F373xx		USART1/USART2/ DFU (USB Device FS)	0x41	0x1FFFF7A6	USART (V3.1) DFU (V2.2)
	STM32F378xx		USART1/USART2/ I2C1	0x50	0x1FFFF7A6	USART (V3.1) I2C (V1.0)
	STM32F302xB(C)/303xB(C)		USART1/USART2/ DFU (USB Device FS)	0x41	0x1FFFF796	USART (V3.1) DFU (V2.2)
	STM32F358xx		USART1/USART2/ I2C1	0x50	0x1FFFF796	USART (V3.1) I2C (V1.0)
	STM32F301xx/302x4(6/8)		USART1/USART2/ DFU (USB Device FS)	0x40	0x1FFFF796	USART (V3.1) DFU (V2.2)
	STM32F318xx		USART1/USART2/ I2C1/ I2C3	0x50	0x1FFFF796	USART (V3.1) I2C (V1.0)
	STM32F303x4(6/8)/334xx/328xx		USART1/USART2/ I2C1	0x50	0x1FFFF796	USART (V3.1) I2C (V1.0)

Figure 9. Embedded bootloaders

STM32 series	Device	Supported serial peripherals	Bootloader ID		Bootloader (protocol) version
			ID	Memory location	
F4	STM32F40xx/41xxx	USART1/USART3/ CAN2/ DFU (USB Device FS)	0x31	0x1FFF77DE	USART (V3.1) CAN (V2.0) DFU (V2.2)
		USART1/USART3/ CAN2 / DFU (USB Device FS) /I2C1/I2C2/I2C3/SPI1/ SPI2	0x90	0x1FFF77DE	USART (V3.1) CAN (V2.0) DFU (V2.2) SPI(V1.1) I2C (V1.0)
	STM32F427xx/437xx	USART1/USART3/ CAN2 /DFU (USB Device FS)	0x30	0x1FFF76DE	USART (V3.1) CAN (V2.0) DFU (V2.2)
	STM32F429xx/439xx	USART1/USART3/ CAN2 /DFU (USB Device FS) / I2C1/I2C2/I2C3	0x70	0x1FFF76DE	USART (V3.1) CAN (V2.0) DFU (V2.2) I2C (V1.0)
		USART1/USART3/ CAN2 / DFU (USB Device FS) / I2C1/I2C2/I2C3/SPI1/ SPI2/ SPI4	0x90	0x1FFF76DE	USART (V3.1) CAN (V2.0) DFU (V2.2) SPI(V1.1) I2C (V1.0)
	STM32F401xB(C)	USART1/USART2/ DFU (USB Device FS)/ I2C1/I2C2/I2C3/ SPI1/SPI2/ SPI3	0xD1	0x1FFF76DE	USART (V3.1) DFU (V2.2) SPI(V1.1) I2C (V1.0)
	STM32F401xD(E)	USART1/USART2/ DFU (USB Device FS)/ I2C1/I2C2/I2C3/ SPI1/SPI2/ SPI3	0xD1	0x1FFF76DE	USART (V3.1) DFU (V2.2) SPI(V1.1) I2C (V1.1)
L0	STM32L05xxx/06xxx	USART1/USART2/SPI 1/ SPI2	0xC0	0x1FF00FFE	USART (V3.1) SPI (V1.1)
L1	STM32L1xxx6(8/B)	USART1/USART2	0x20	0x1FF00FFE	USART (V3.0)
	STM32L1xxx6(8/B)A	USART1/USART2	0x20	0x1FF00FFE	USART (V3.1)
	STM32L1xxxC	USART1/USART2/ DFU (USB Device FS)	0x40	0x1FF01FFE	USART (V3.1) DFU (V2.2)
	STM32L1xxxD	USART1/USART2/ DFU (USB Device FS)	0x45	0x1FF01FFE	USART (V3.1) DFU (V2.2)
	STM32L1xxxE	USART1/USART2/ DFU (USB Device FS)	0x40	0x1FF01FFE	USART (V3.1) DFU (V2.2)

Figure 10. Embedded bootloaders

4 JTAG/SWD

4.1 Introduction

Host Target interface Figure 11 JTAG / SWD debug tool Host PC STM32 .

(device SWD device .)

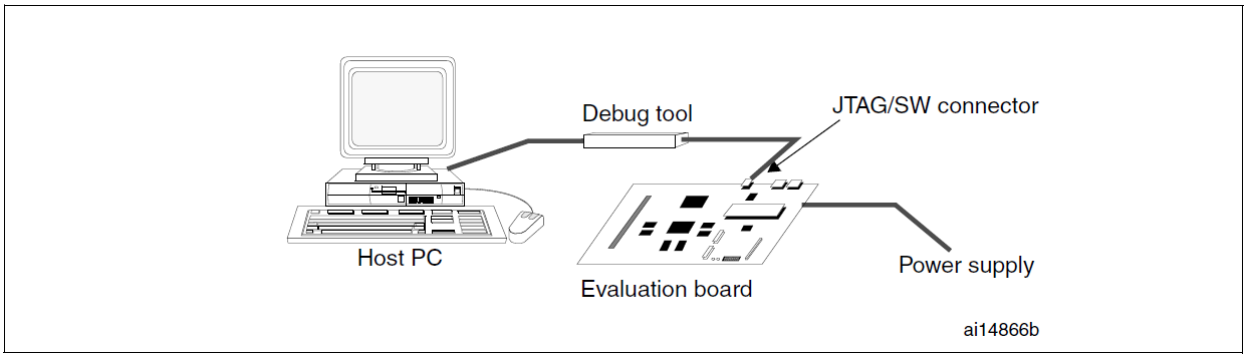

Figure 11. Host to board connection

4.2 SWJ debug port (serial wire and JTAG)

STM32 ARM standard CoreSight debug port SWJ-DP . SWJ-DP JTAG-DP(5pin) SW-DP(2pin) .

.

- Table 6 SWJ-DP pin .

SWJ-DP pin name	JTAG debug port		SW debug port		Pin assignment
	Type	Description	Type	Debug assignment	
JTMS/SWDIO	I	JTAG test mode selection	I/O	Serial wire data input/output	PA13
JTCK/SWCLK	I	JTAG test clock	I	Serial wire clock	PA14
JTDI	I	JTAG test data input	-	-	PA15
JTDO/TRACESWO	O	JTAG test data output	-	TRACESWO if async trace is enabled	PB3
JNTRST	I	JTAG test nReset	-	-	PB4

Table 6. Debug pin assignmment

- Table 7 debugging pin .

Available Debug ports	SWJ I/O pin assigned				
	PA13 / JTMS/ SWDIO	PA14 / JTCK/ SWCLK	PA15 / JTDI	PB3 / JTDO	PB4/ JNTRST
Full SWJ (JTAG-DP + SW-DP) - reset state	X	X	X	X	X
Full SWJ (JTAG-DP + SW-DP) but without JNTRST	X	X	X	X	
JTAG-DP disabled and SW-DP enabled	X	X			
JTAG-DP disabled and SW-DP disabled	Free to be configured as alternate functions				

Table 7. SWJ pin availability

- Figure 12 JTAG connector .

  JTAG connector debugger ,

  debugger user manual .

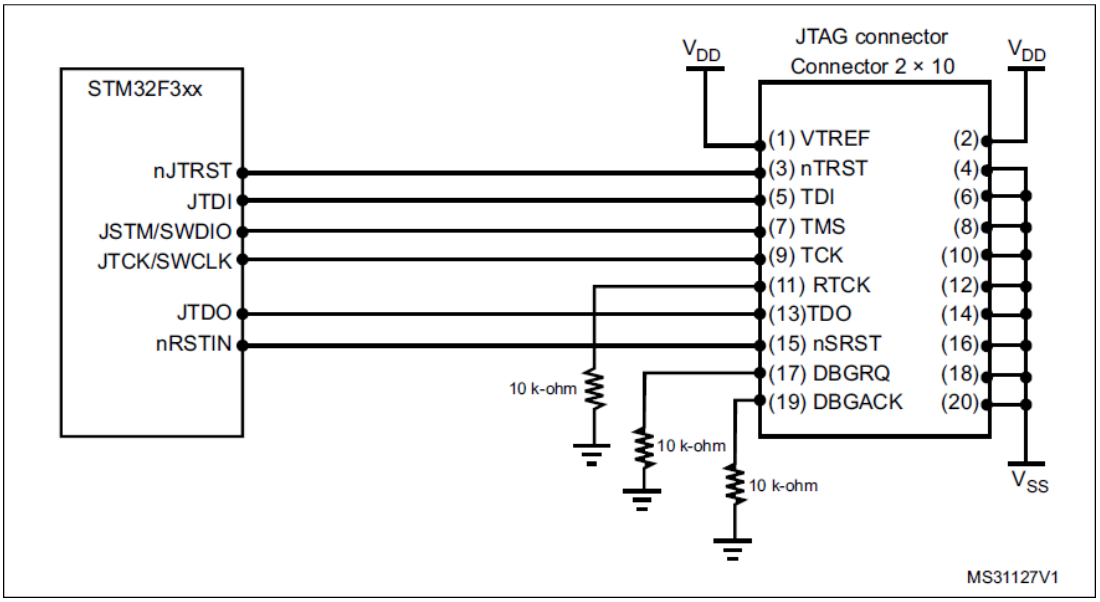

Figure 12. JTAG connector implementation

- Table 8 ST-Link debugger JTAG connector pin description .

Table 8. ST-Link V2 JTAG connecter pin description

Pin no.	ST-LINK/V2 connector (CN3)	ST-LINK/V2 function	Target connection (JTAG)	Target connection (SWD)
1	VAPP	Target VCC	MCU VDD(1)	MCU VDD(1)
2				
3	TRST	JTAG TRST	JNTRST	GND(2)
4	GND	GND	GND(3)	GND(3)
5	TDI	JTAG TDO	JTDI	GND(2)
6	GND	GND	GND(3)	GND(3)
7	TMS_SWDIO	JTAG TMS, SW IO	JTMS	SWDIO
8	GND	GND	GND(3)	GND(3)
9	TCK_SWCLK	JTAG TCK, SW CLK	JTCK	SWCLK
10	GND	GND	GND(3)	GND(3)
11	NC	Not connected	Not connected	Not connected
12	GND	GND	GND(3)	GND(3)
13	TDO_SWO	JTAG TDI, SWO	JTDO	TRACESWO(4)
14	GND	GND	GND(3)	GND(3)
15	NRST	NRST	NRST	NRST
16	GND	GND	GND(3)	GND(3)
17	NC	Not connected	Not connected	Not connected
18	GND	GND	GND(3)	GND(3)
19	VDD	VDD (3.3V)	Not connected	Not connected
20	GND	GND	GND(3)	GND(3)

1. The power supply from the application board is connected to the ST-LINK/V2 debugging and programming board to ensure signal compatibility between both boards.
2. Connect to GND for noise reduction on the ribbon
3. At least one of this pin must be connected to the ground for correct behavior (connecting all of them is recommended)
4. Optional: for Serial Wire Viewer (SWV) trace

5 Recommendations

5.1 PCB

PCB power ground multilayer
. application multilayer
ground pattern PCB
.

5.2 Ground and power supply

power ground pattern .
power supply loop ground pattern
. Supply loop , loop antenna EMI
EMI . PCB layout ground
pattern EMI .

5.3 Decoupling

MCU power VDD/VSS pair application
10nF~100nF decoupling capacitor . device
4.7uF capacitor .

- Figure 13 decoupling capacitor device
.

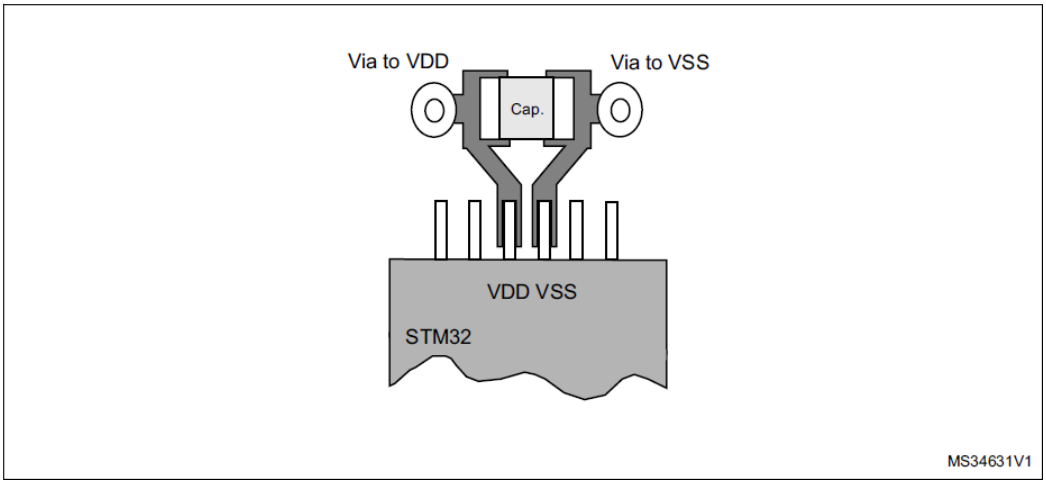

Figure 13. Typical layout for VDD/VSS pair

5.4 Unused I/O

EMC I/O pull-up/pull-down

logic ‘0’ ‘1’ .

application I/O analog input

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